

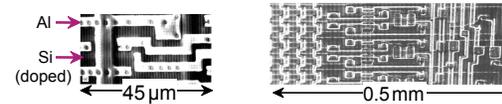
Electrical Properties

ISSUES TO ADDRESS...

- How are electrical conductance and resistance characterized? (What effects conductance?)
- What are the physical phenomena that distinguish conductors, semiconductors, and insulators?
- For metals, how is conductivity affected by imperfections, temperature, and deformation?
- For semiconductors, how is conductivity affected by impurities (doping) and temperature?

View of an Integrated Circuit

- Scanning electron micrographs of an IC:



- A dot map showing location of Si (a semiconductor):
 - Si shows up as light regions.
 - & dark region is Al wiring



Electrical Conduction

- Ohm's Law:

$$V = IR$$

voltage drop (volts = J/C) current (amps = C/s) resistance (Ohms)
 C = Coulomb

- Resistivity, ρ :
 - a material property that is independent of sample size and geometry

$$R = \frac{\rho L}{A}$$

current flow path length cross-sectional area of current flow

$$\rho = \frac{RA}{\ell}$$

- Conductivity, σ

$$\sigma = \frac{1}{\rho}$$

Electrical Properties

- Which will have the greater resistance?

$$R_1 = \frac{2\rho\ell}{\pi\left(\frac{D}{2}\right)^2} = \frac{8\rho\ell}{\pi D^2}$$

$$R_2 = \frac{\rho\ell}{\pi\left(\frac{2D}{2}\right)^2} = \frac{\rho\ell}{\pi D^2} = \frac{R_1}{8}$$

- Analogous to flow of cars on road
- Resistance depends on sample geometry and size.
- Resistivity of independent of sample geometry

Definitions

Further definitions

$J = \sigma \epsilon$

← another way to state Ohm's law

J = current density = $\frac{\text{current}}{\text{surface area}} = \frac{I}{A}$ like a flux

ϵ = electric field potential = V/ℓ

$$J = \sigma(V/\ell)$$

↑ Electron flux
 ↑ conductivity
 ↑ voltage gradient

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Chapter 18 - 5

Conductivity: Comparison

Room temperature values in $(\Omega \cdot \text{m})^{-1}$

METALS	conductors	CERAMICS
Silver	6.8×10^7	Soda-lime glass 10^{-10} - 10^{-11}
Copper	6.0×10^7	Concrete 10^{-9}
Iron	1.0×10^7	Aluminum oxide $<10^{-13}$
SEMICONDUCTORS	semiconductors	POLYMERS
Silicon	4×10^{-4}	Polystyrene $<10^{-14}$
Germanium	2×10^0	Polyethylene 10^{-15} - 10^{-17}
GaAs	10^{-6}	
		insulators

Selected values from Tables 18.1, 18.3, and 18.4, Callister & Rethwisch 9e.

Example: Conductivity Problem

What is the minimum diameter (D) of the Cu wire so that $V < 1.5$ V?

$R = \frac{\ell}{A\sigma} = \frac{V}{I}$

$\frac{\pi D^2}{4} \rightarrow A$
 $\ell = 100 \text{ m}$
 $\sigma = 6.07 \times 10^7 \text{ (Ohm-m)}^{-1}$
 $V < 1.5 \text{ V}$
 $I = 2.5 \text{ A}$

Solve to get $D > 1.87 \text{ mm}$

Electron Drift

$v_{avg} = \mu E$

Electrons are scattered and drift *slowly* in one direction (1.2 in./min in Cu) due to the E field.

However electrical signal “appear” to travels at about 2/3 the speed of light.

As one electron is pushed into “full” pipe, an electron is pushed out the other end.

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$$\sigma = n |e| \mu_e$$

σ - Conductivity
 n - # of free electrons/VOL
 e - 1.6×10^{19} C
 μ_e - Electron Mobility

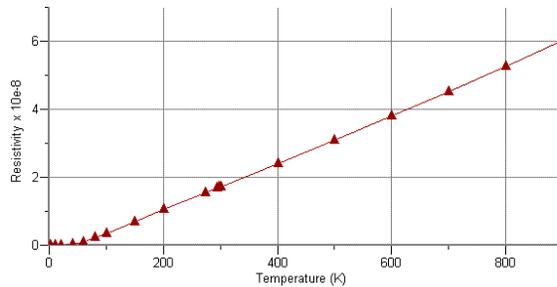
Matthiessen's Rule: The total resistivity of a material is the sum of the contributions from thermal vibrations, impurities, and plastic deformation

$$\rho_{total} = \rho_t + \rho_i + \rho_d$$

t - Thermal Vibrations -- temperature
 i - Impurities -- wt% impurity
 d - Deformation -- %CW

Resistance rises linearly with temperature when $T > -200$ °C

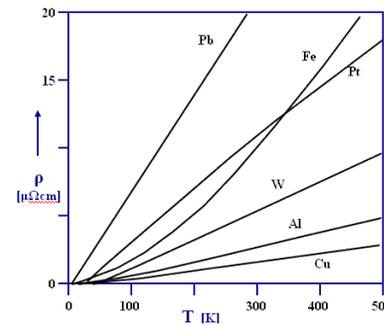
Resistivity of Copper



$$\rho_t = \rho_0 + aT$$

Resistance vs. temp for other metals

$$\rho_t = \rho_0 + aT$$



Metals: Influence of Temperature and Impurities on Resistivity

- Presence of imperfections increases resistivity
 - grain boundaries
 - dislocations
 - impurity atoms
 - vacancies

These act to scatter electrons so that they take a less direct path.

- Resistivity increases with:
 - temperature
 - wt% impurity
 - %CW

$$\rho = \rho_{\text{thermal}} + \rho_{\text{impurity}} + \rho_{\text{deformation}}$$

Fig. 18.8, Callister & Rethwisch 9e. [Adapted from J. O. Linde, Ann. Physik, 5, 219 (1932); and C. A. Wert and R. M. Thomson, Physics of Solids, 2nd edition, McGraw-Hill Book Company, New York, 1970.]

Estimating Conductivity

- Question:
 - Estimate the electrical conductivity σ of a Cu-Ni alloy that has a yield strength of 125 MPa.

Adapted from Fig. 18.9, Callister & Rethwisch 9e.

Adapted from Fig. 7.16(b), Callister & Rethwisch 9e.

From step 1:

$$C_{\text{Ni}} = 21 \text{ wt\% Ni}$$

$$\rho = 30 \times 10^{-8} \text{ Ohm-m}$$

$$\sigma = \frac{1}{\rho} = 3.3 \times 10^6 \text{ (Ohm-m)}^{-1}$$

Electron Energy Band Structures

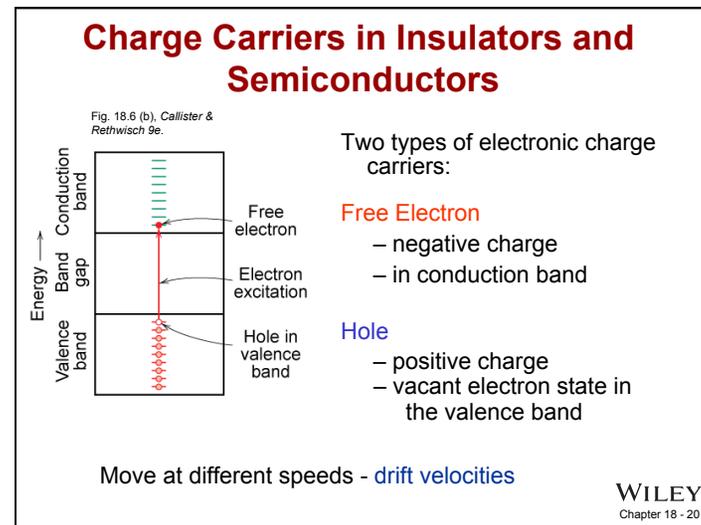
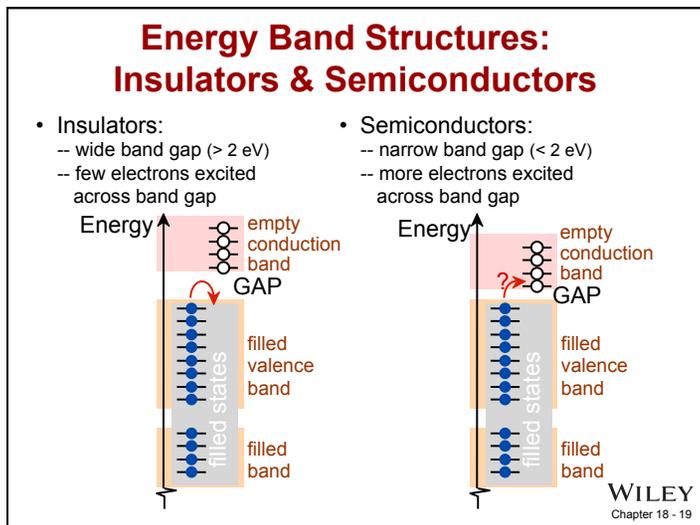
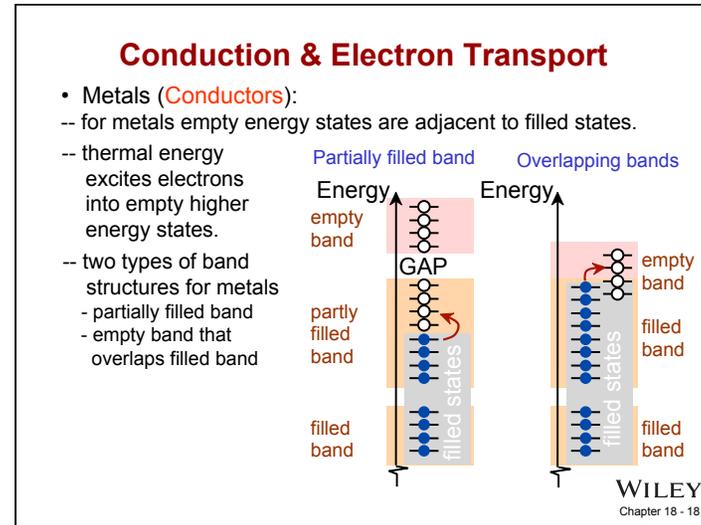
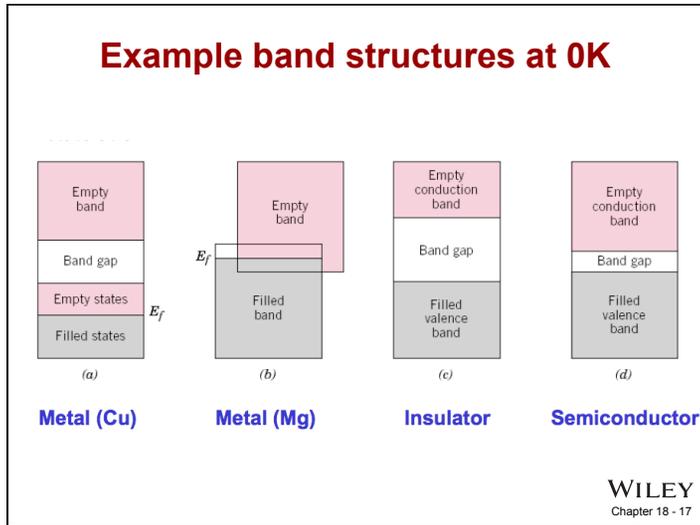
Adapted from Fig. 18.2, Callister & Rethwisch 9e.

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Band Structure Representation

Fig. 18.3, Callister & Rethwisch 9e.

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Intrinsic Semiconductors

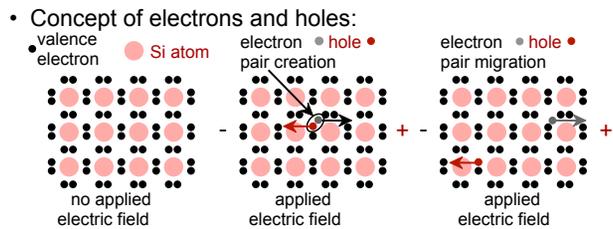
- Pure material semiconductors: e.g., silicon & germanium
 - Group IVA materials
- Compound semiconductors
 - III-V compounds
 - Ex: GaAs & InSb
 - II-VI compounds
 - Ex: CdS & ZnTe
 - The wider the electronegativity difference between the elements the wider the energy gap.

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Periodic Table of the Elements

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Chapter 18 - 22

Intrinsic Semiconduction in Terms of Electron and Hole Migration



- Electrical Conductivity given by:

$$\sigma = n|e|\mu_e + p|e|\mu_h$$

electrons/m³ # holes/m³ electron mobility hole mobility

Adapted from Fig. 18.11, Callister & Rethwisch 9e.

Number of Charge Carriers

Intrinsic Conductivity

$$\sigma = n|e|\mu_e + p|e|\mu_h$$

- for intrinsic semiconductor $n = p = n_i$

$$\therefore \sigma = n_i |e| (\mu_e + \mu_h)$$

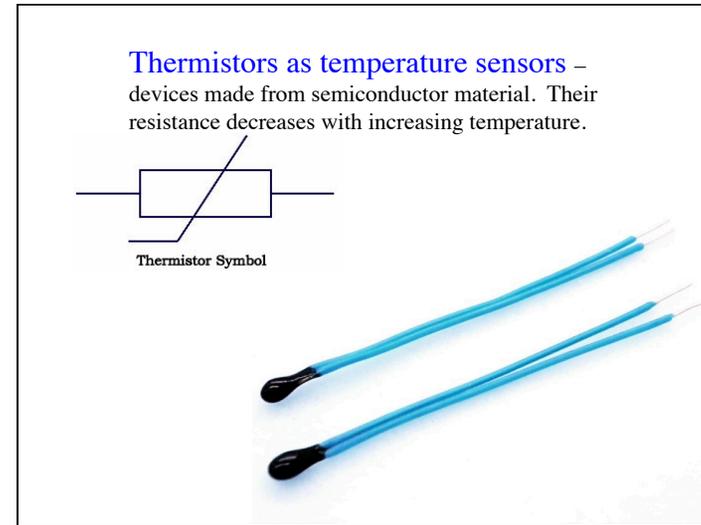
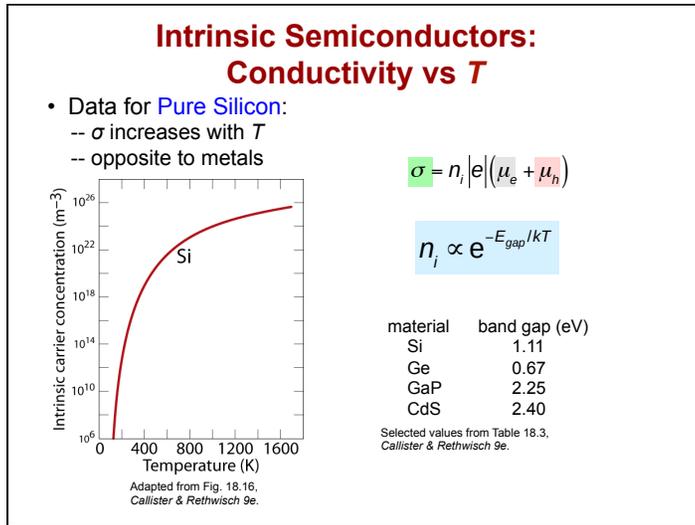
- Ex: GaAs

$$n_i = \frac{\sigma}{|e|(\mu_e + \mu_h)} = \frac{10^{-6} (\Omega \cdot \text{m})^{-1}}{(1.6 \times 10^{-19} \text{C})(0.85 + 0.45 \text{ m}^2/\text{V} \cdot \text{s})}$$

For GaAs $n_i = 4.8 \times 10^{24} \text{ m}^{-3}$

For Si $n_i = 1.3 \times 10^{16} \text{ m}^{-3}$

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Comparing Si to Cu at room temp.

- $\mu_{Cu} = 30 \text{ cm}^2/\text{V-S}$
- $n_{Cu} = 10^{29} /\text{cm}^2$
- $\mu_{Si} = 1400 \text{ cm}^2/\text{V-S}$
- $n_{Si} = 10^{16} /\text{cm}^2$

Electrons are 50 times more mobile in Si than in Cu but there are many more free electrons in Cu, therefore Cu is 200,000,000,000 times less resistive compared to copper.

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Chapter 18 - 28

Intrinsic vs Extrinsic Conduction

- Intrinsic:**
 - case for pure Si
 - # electrons = # holes ($n = p$)
- Extrinsic:**
 - electrical behavior is determined by presence of impurities that introduce excess electrons or holes
 - $n \neq p$
- n-type Extrinsic:** ($n \gg p$) • **p-type Extrinsic:** ($p \gg n$)

Phosphorus atom

$\sigma \approx n | e | \mu_e$

no applied electric field

Boron atom

$\sigma \approx p | e | \mu_h$

no applied electric field

Adapted from Figs. 18.12(a) & 18.14(a), Callister & Rethwisch 9e.

Periodic Table of the Elements

Extrinsic Semiconductors: Conductivity vs. Temperature

Data for **Doped Silicon**:
 σ increases with doping
 Reason: dopants donate charge carriers.
 Conduction electrons = # of dopant ions.

- Comparison: **intrinsic** vs **extrinsic** conduction...
- extrinsic doping level: $10^{21}/m^3$ of a *n*-type donor impurity (such as P).
- for $T < 100$ K: "freeze-out", thermal energy insufficient to excite electrons.
- for 150 K $< T < 450$ K: "extrinsic"
- for $T \gg 450$ K: "intrinsic"

Adapted from Fig. 18.17, Callister & Rethwisch 9e, (From S. M. Sze, Semiconductor Devices, Physics and Technology, Copyright © 1985 by Bell Telephone Laboratories, Inc. Reprinted by permission of John Wiley & Sons, Inc.)

Factors That Affect Carrier Mobility

Calculate the room-temperature electrical conductivity of silicon that has been doped with $2 \times 10^{23} m^{-3}$ of arsenic atoms.

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$$\sigma = n | e | \mu_e = (2 \times 10^{23} m^{-3})(1.602 \times 10^{-19} C)(0.05 m^2 / V-s) = 1600 (\Omega - m)^{-1}$$

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p-n Rectifying Junction

- Allows flow of electrons in one direction only (e.g., useful to convert alternating current to direct current).
- Processing: diffuse P into one side of a B-doped crystal.

-- No applied potential: no net current flow.

-- Forward bias: carriers flow through p-type and n-type regions; holes and electrons recombine at p-n junction; current flows.

-- Reverse bias: carriers flow away from p-n junction; junction region depleted of carriers; little current flow.

Adapted from Fig. 18.21, Callister & Rethwisch 9e.

Properties of Rectifying Junction

Fig. 18.22, Callister & Rethwisch 9e.

Fig. 18.23, Callister & Rethwisch 9e.

Junction Transistor

Fig. 18.24, Callister & Rethwisch 9e.

P N P
EMITTER BASE COLLECTOR

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MOSFET Transistor Integrated Circuit Device

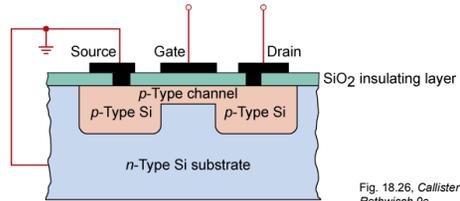
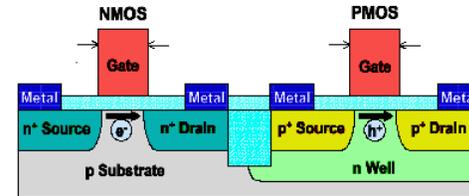


Fig. 18.26, Callister & Rethwisch 9e.

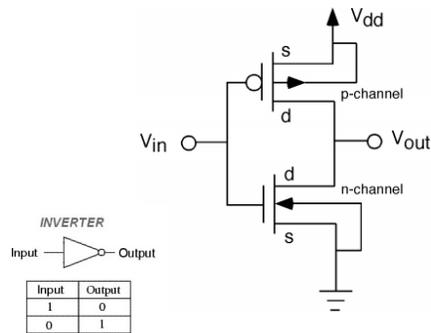
- MOSFET (metal oxide semiconductor field effect transistor)
- Integrated circuits – “state of the art” 50 nm channel width
 - ~ 5,000,000,000 transistors on chip
 - chips formed one layer at a time

CMOS → nMOS + pMOS

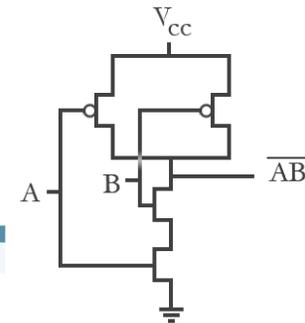
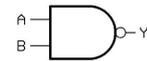


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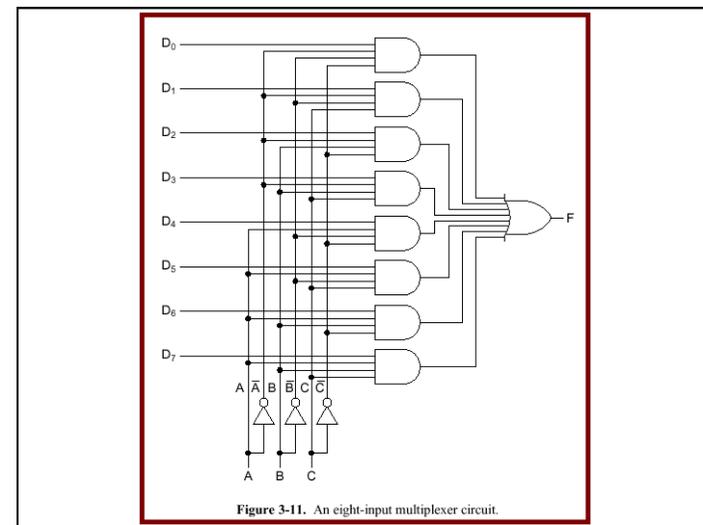
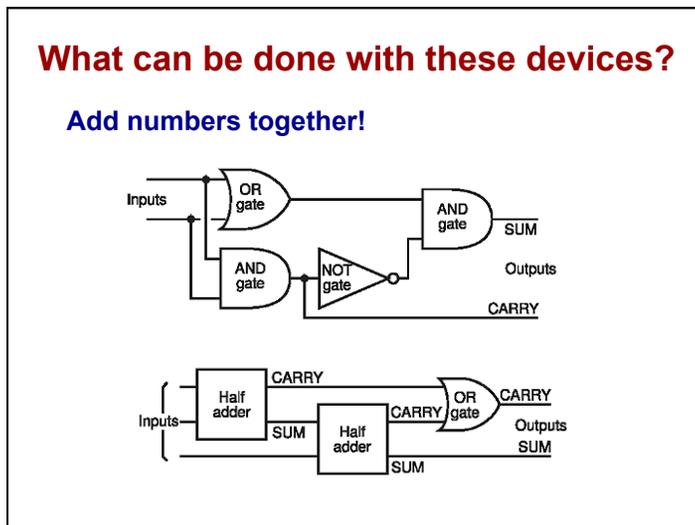
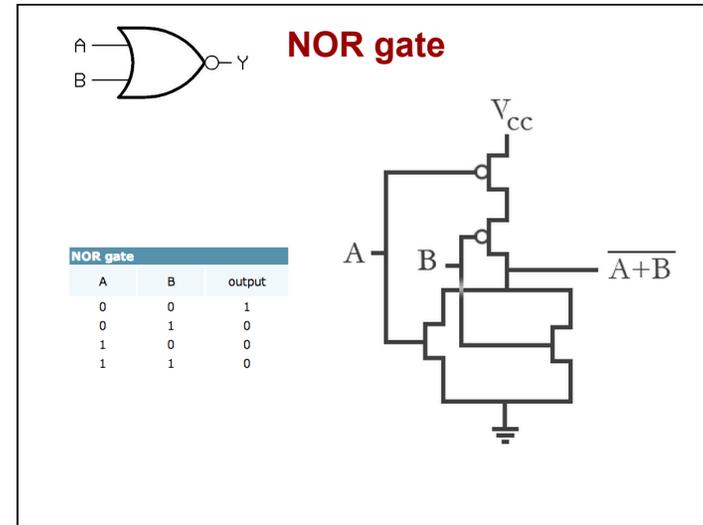
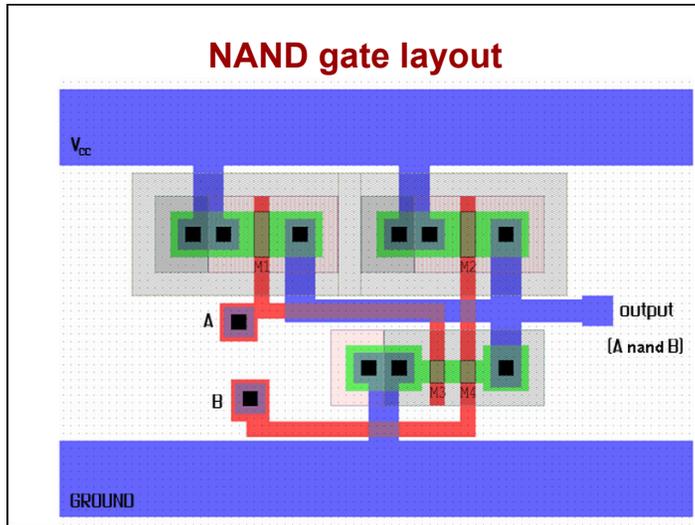
Building simple devices – The Inverter

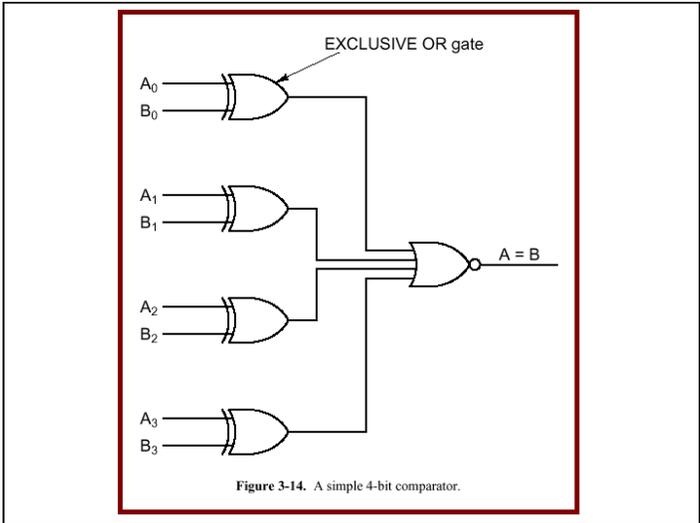
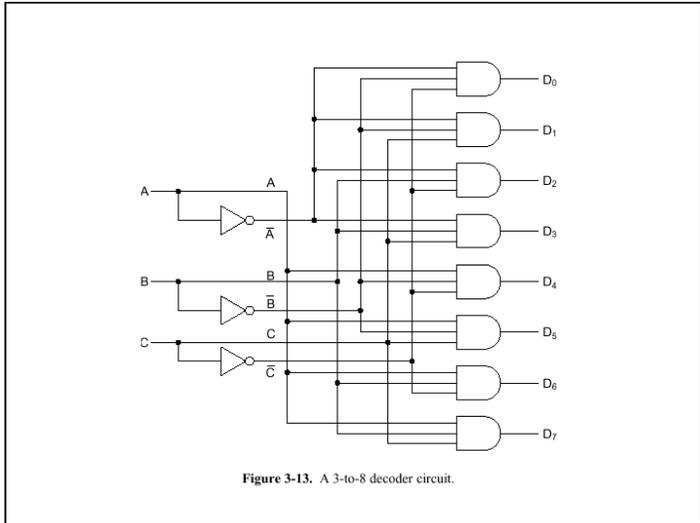


The NAND Gate



NAND gate		
A	B	output
0	0	1
0	1	1
1	0	1
1	1	0





Why can we build devices with semiconductors?

- **Semiconductors are neither good insulators or good conductors.**
- **We can select specific, small regions to be electrically conductive for either holes or electrons.**
- **Other regions can be made insulating by growing an oxide film**
- **The electrical properties of the conductive regions can be altered by applying a positive or negative voltage.**

- **The number of charge carriers in an extrinsic semiconductor (n) is controlled by the number of dopants when temperature is between 150- 450 K.**
- **Using dopants we can create regions within si that have an engineered value for conductivity.**
- **Certain regions can be made conductive for certain types of charge carriers by applying a voltage.**

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Chapter 18 - 48

Summary

- Electrical *conductivity* and *resistivity* are:
 - material parameters
 - geometry independent
- Conductors, semiconductors, and insulators...
 - differ in range of conductivity values
 - differ in availability of electron excitation states
- For metals, *resistivity* is increased by
 - increasing temperature
 - addition of imperfections
 - plastic deformation
- For pure semiconductors, *conductivity* is increased by
 - increasing temperature
 - doping [e.g., adding B to Si (*p*-type) or P to Si (*n*-type)]